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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10038870	01/08/2002	716	5	2825	Dirk

* APPLICANTS: Johannsen Peer;

CONTINUING DATA VERIFIED:

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** FOREIGN APPLICATIONS VERIFIED:

GERMANY 10100433.8 01/08/2001

EUROPEAN PATENT OFFICE (EPO) 01108653.5 04/05/2001

PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed 35 USC 119 conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO 1454.1210
Verified and Acknowledged Examiner's initials		
TITLE : Method of circuit verification in digital design		

U.S. DEPT. OF COMM /PAT & TM-PTO-438L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figa.Drwg.
Primary Examiner		Print Fig.	
PREPARED FOR ISSUE		Application Examiner	
TERMINAL DISCLAIMER			
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